PROCESSING, FABRICATION, AND DEMONSTRATION OF HTS INTEGRATED MICROWAVE CIRCUITS

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Submitted by:

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R&D STATUS REPORT

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Short Title of Work: Processing, Fabrication, and Demonstration of HTS Integrated Microwave Circuits

Reporting Period: 7/26/93 to 10/24/93

DESCRIPTION OF PROGRESS

TASK 1.0: COMPARATIVE TECHNOLOGY ASSESSMENT

This task is essentially complete, but we are continuing to monitor progress in other technologies as they relate to the goals of this program.

TASK 2.1: INTEGRATED SUBSYSTEM SPECIFICATIONS

Part of this task is to determine how the HTS channelized filterbank can be most effectively demonstrated. Preferably the demonstration should be accomplished in the context of an actual ESM receiver rather than as a laboratory demonstration using laboratory instrumentation. We have identified a demonstration vehicle which will provide this capability. Westinghouse, using internal R&D funding, has developed and demonstrated a wideband channelized receiver with twenty, 100 MHz channels that operates over the 3 to 5 GHz frequency range. This receiver is capable of detecting and correctly determining the frequency of up to three simultaneous signals, even when they have simultaneous leading edges.

The HTS filterbank being developed under this program is designed to operate right in the middle of this frequency range (4 GHz) and it has been determined that the filter characteristics and parameters of the two channelizers are similar enough to be compatible with the encoder algorithms. The channelized receiver's log video detectors, A/Ds, and digital encoder are also compatible with the HTS channelizer design.

Thus the components for a demonstration of the HTS filterbank can be made available and a realistic demonstration can be conducted at a very reasonable cost.

TASK 2.2: FUNCTIONAL COMPONENT AND SUBSYSTEM DESIGN, FABRICATION AND TESTING

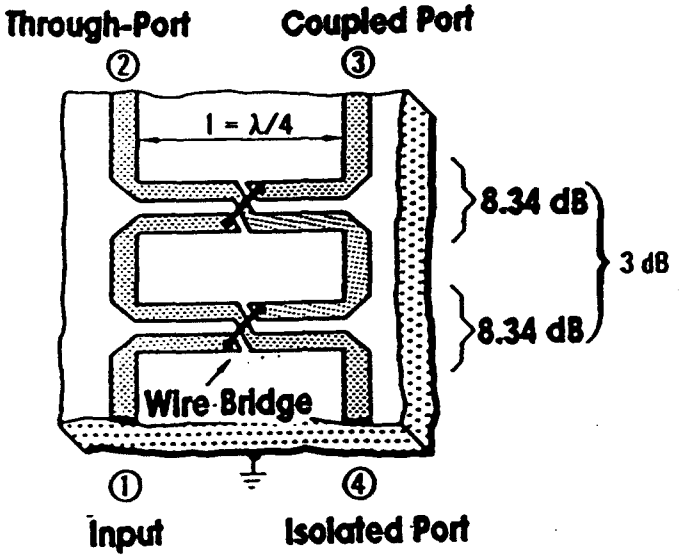
Filterbanks

- Wide-Band Coupler Design

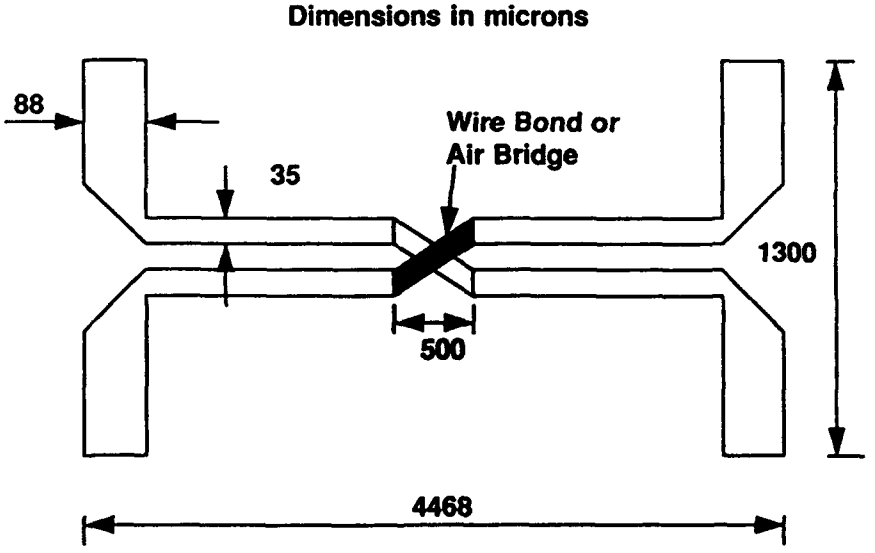
A wide band 90° coupler has been designed. This component is needed for the implementation of the HTS filterbank. Our original plans called for a Lange coupler design. However, due to the high dielectric constant of the LAO substrate, a 3 dB Lange coupler would have very narrow and long lines, posing a high risk on its fabrication. For example, a 4-finger Lange coupler requires lines 1.7 μm wide and almost 0.5 cm long, with 9.4 μm spacings. This was considered to be too risky from a fabrication yield standpoint. Instead, two 8.34 dB quarter-wave couplers in tandem will be used. The coupler layout is shown schematically in Figure 1(a). Figure 1(b) shows the designed dimensions for each coupler for a LAO substrate 0.025-cm (10 mils) thick. The separation between couplers is not critical, only that it be sufficiently wide to avoid spurious interactions between couplers. Thus, the total coupler is approximately as wide as the branch-line hybrid we have used to date on the parallel HTSSE-II program, but about half as long. The tandem coupler was designed using the microwave circuit design software Touchstone and later adjusted using the electromagnetic analysis software em™, from Sonnet. The analyzed performance is shown in Figures 2(a) and 2(b). Refer to Figure 1(a) for the port labels.

- Filter Design

All the filterbank technology developed in this program to date has been directly demonstrated in the parallel Navy program HTSSE-II. The filterbank requirements of this ONR/ARPA program are somewhat different in that, instead of Chebychev filter characteristics, a quasi-$\cos^3$ passband shape is to be used in order to demonstrate the technology in EW system applications. These filters have been electrically designed, and their characteristics analyzed in the context of an EW channelized receiver. This has been

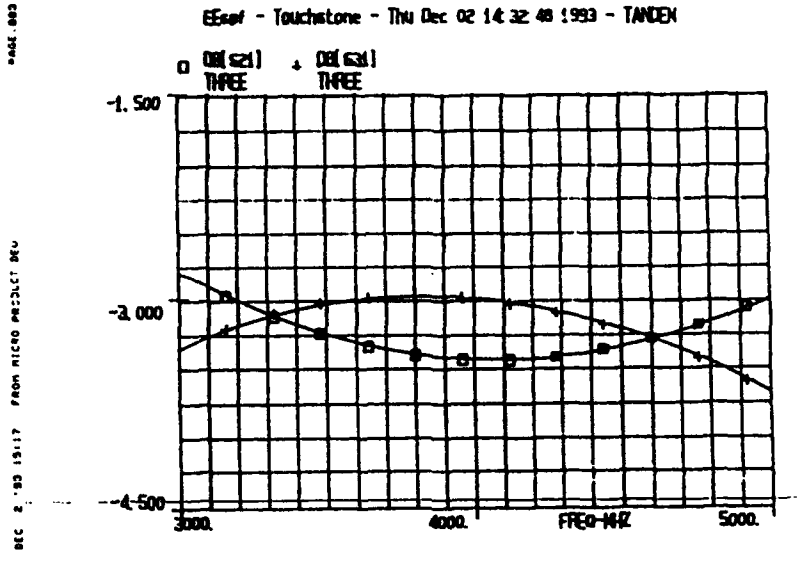


(a)

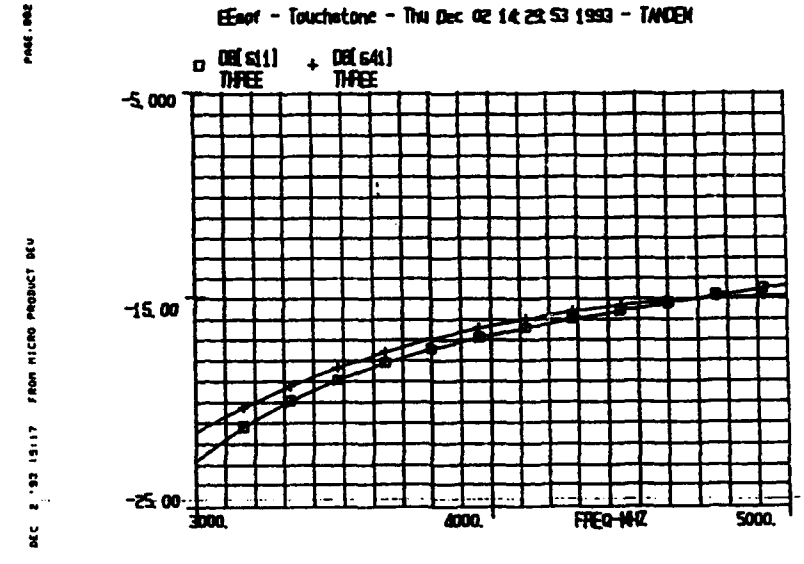


(b)

Figure 1. Tandem couplers. Each is a 8.34-dB parallel-coupled line coupler. In tandem they provide a 3 dB coupler over almost an octave bandwidth. (a) Schematic layout. (b) Dimensions for each coupler.



(a)



(b)

Figure 2. Design and Sonnet analysis of the tandem coupler performance.

previously reported in our interim report covering the period between July 1991 and July 1992. The geometrical design of the first channel is now nearly complete. This a seven-pole, quarter-wave parallel-coupled section filter on a 0.025-cm thick LAO substrate. The design is complicated by the fact that the conventional design software is inadequate to perform this task, as explained in our last quarterly report. A design procedure is being developed in which Sonnet is included in the design loop. Although the procedure is not yet optimized for speed, it is possible to obtain suitable designs with it. The steps employed are the following:

a) Design the filter with Touchstone™ (or equivalent) to obtain a first set of coupling gaps and average coupling lengths.

b) Using Sonnet™ at frequency points of interest construct a table of coupling gaps versus frequency for the average coupling length obtained in step a).

c) Knowing the required couplings from the impedance model of the filter, interpolate the table to find the corresponding gap for each section.

d) Analyze the resulting filter using Sonnet. This is the first iteration. The center frequency is usually different from that desired.

e) From the frequency offset, compute a length correction for each coupling section.

f) Repeat step b) using the new average coupling length.

g) Repeat steps c), d) and e).

This design procedure is still being refined but has yielded reasonably good designs for the Chebychev filters of the HTSSE-II program. Experimental results on these filters will be obtained in the next reporting period.

- Fabrication and Testing of Thin-Film rf Terminations

In the previous report, the need for an integrated 50 Ω load resistor to properly terminate the 180° out-of-phase port from each filterbank channel was described. A process for fabricating these thin film resistors was defined and a mask set to test the fabrication process was designed in the previous period as well. During the current reporting period, this mask set was used in processing two two-inch wafers to produce thin-film loads and associated test patterns. A diagram of the chip layout for this mask set is given in Figure 3. Twelve thin-film load structures from these two wafers were tested over the frequency range 2 to 6 GHz. Also measured after processing were the YBCO surface resistance at 10 GHz and dc properties of YBCO and the load resistor material.

The starting substrate for fabricating the components shown in Figure 3 was a $LaAlO_3$ wafer (0.05 cm thick) on which an epitaxial layer of YBCO (0.4 μm thick) had been grown by off-axis sputtering at Westinghouse STC. The processing sequence proceeded as follows. Au contacts to the YBCO were defined by lift-off with 200 nm Au deposited by sputtering. The contacts were annealed in flowing oxygen for one hour at 550° C to promote adhesion and to provide sufficiently low contact resistance. The YBCO was patterned as transmission lines to the thin-film loads and for various test structures by Ar ion milling. The resistor structure, also defined by lift-off, consisted of 86 nm Mo capped with 10 nm Ti and had a target sheet resistance of 1.0 Ω/□ at 77 K. The Ti capping layer serves to protect the Mo resistor material from oxidation by atmospheric oxygen. The final layer on the front of the substrate was sputtered Ti/Au (20 nm/200 nm), defined by lift-off, where the Ti promotes adhesion and the Au provides a surface to which wire bonds can be made for the test patterns. This layer was used to connect one end of the thin-film load resistor to the YBCO transmission line and the other end of the resistor to the Ti/Au capacitor electrode which provides an ac path to the ground plane on the back of the wafer. The ground plane was created by sputter-depositing Cr/Au (20 nm/200 nm) on the $LaAlO_3$ substrate and then plating an additional 2 μm of Au onto the sputtered Au. The wafer was then sawed into eleven chips for testing.

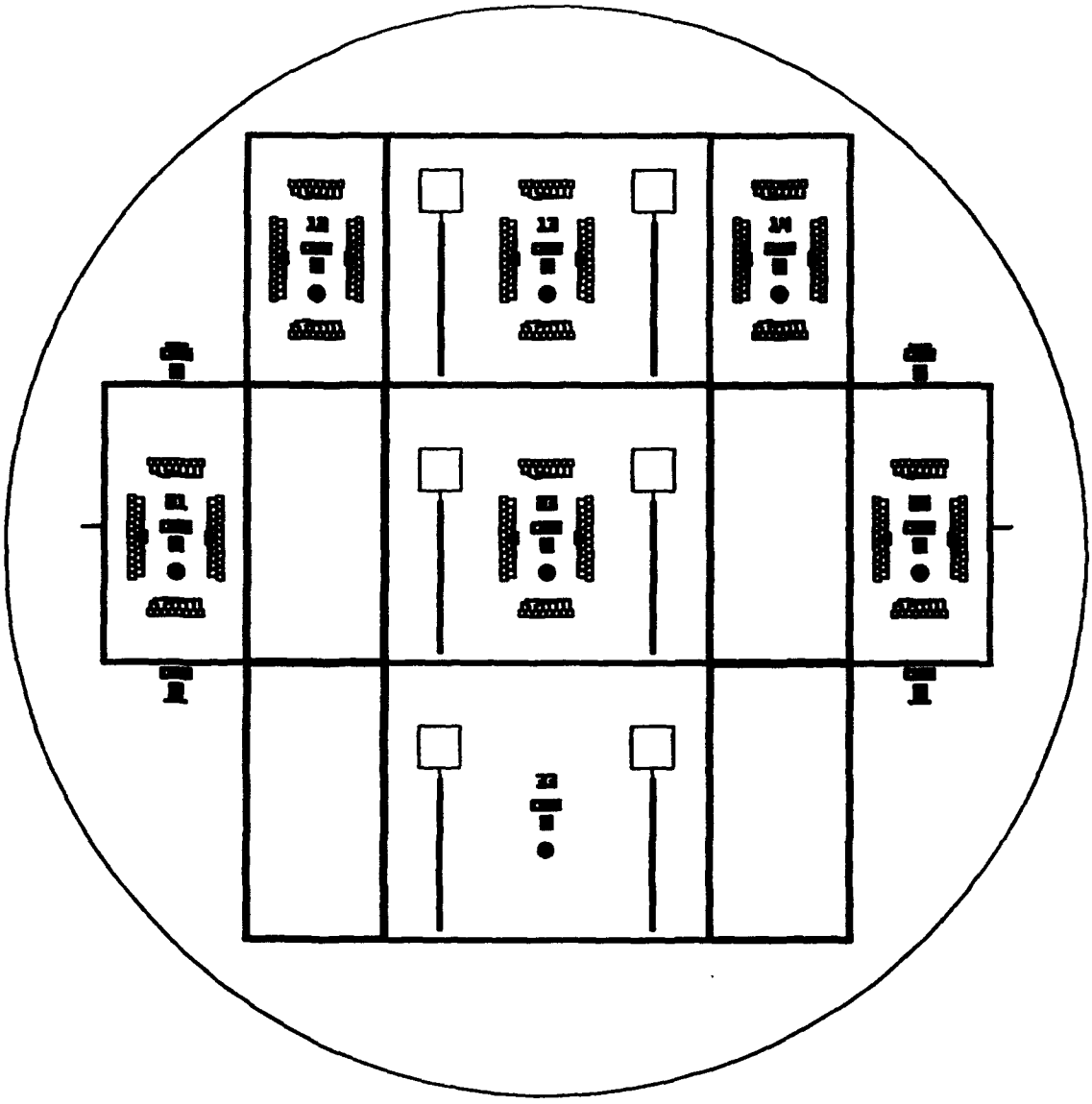


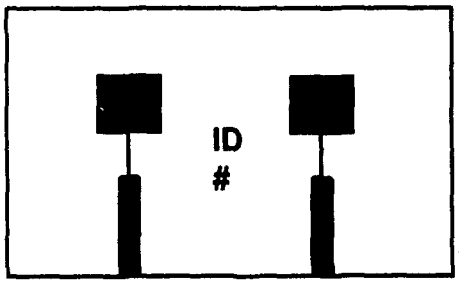
Figure 3. Diagram of layout of thin-film load structures (three chips in center column), test pieces for measurement of surface resistance after processing (four blank rectangular chips), and test patterns for measuring dc properties of YBCO and the thin-film Mo/Ti resistors (remaining four chips) on a two-inch wafer.

Measurements of the reflection coefficient (S11) for all twelve thin film loads from the two wafers indicated that these loads were performing adequately as termination resistors for the out-of-phase port. The measurements are tabulated in Table 1 as the magnitude of the S11 coefficient given as a range between 2 and 6 GHz and at 4 GHz. These results are quite adequate for providing a termination to leakage signals at the out-of-phase port of the output 90° coupler in each channel.

However, two significant problems surfaced during the processing of these two wafers. The more serious problem is the contamination of the YBCO by the plating solution during the Au plating of the ground plane. The front (YBCO) side of the wafer was protected from the plating solution by a double layer of photoresist. Plating was done using a cyanide-based commercial plating bath (Sel-Rex Pur-A-Gold 401) at 50° C with a plating current of 10 mA for 60 minutes. The photoresist was unable to withstand attack by the heated plating bath for this extended time and broke down in numerous small (≈ 3 μm) regions. This resulted in damage to the YBCO in these localized areas as seen with an optical microscope or with an SEM. As described later, this problem was solved by optimizing the plating conditions in subsequent runds. The second problem involved the inability to lift off all sputtered Au prior to the contact anneal. In cases where isolated small islands of photoresist were defined, such as the interior of the letter "O" in a label or the region between very finely spaced (< 2 μm) lines in a lithography test pattern, the sputtered Au effectively encapsulated and sealed these photoresist islands, thereby preventing the photoresist solvent from dissolving these islands during the lift-off step. Consequently, some photoresist was trapped beneath Au on the wafer during the Au anneal at 550° C. This trapped photoresist could have been released during the anneal and acted as a source of contamination for the YBCO.

Measurements of dc properties of the YBCO film using test chips from the thin-film load wafer confirmed that the YBCO had been degraded electrically. The room temperature resistivity was 640 $\mu\Omega$-cm, approximately twice the value typically obtained for as-deposited YBCO. The critical temperature was 79.5 K, approximately 7 K lower

Table 1. Thin-Film Load rf Measurements



YBCO Wafer	Pkg.	Chip #	Load	Mag(S11) (dB) 2 - 6 GHz	Mag(S11) (dB) 4 GHz
W93-020	FP-02	13	A	10 <Mag(S11)< 26	26
			B	15 <Mag(S11)< 21	17
		23	A	13 <Mag(S11)< 22	21
			B	13 <Mag(S11)< 20	17
	FP-03	33	A	13 <Mag(S11)< 20	20
			B	14 <Mag(S11)< 19	17
W93-021	FP-03	13	A	8 <Mag(S11)< 17	14
			B	15 <Mag(S11)< 20	17
		23	A	14 <Mag(S11)< 17	15
			B	13 <Mag(S11)< 16	14
		33	A	13 <Mag(S11)< 14	13
			B	12 <Mag(S11)< 15	15

than desired, while the critical current density at 73 K was 2.5×10^5 A/cm^2, approximately one-fourth the expected value. These three values are consistent with a degraded YBCO film, probably a consequence of its contact with the plating solution and/or the presence of trapped photoresist on the wafer during the contact anneal. The sheet resistance of the Mo/Ti resistor was 2.24 Ω/□ at room temperature and 1.18 Ω/□ at 72 K, a value which would give an acceptable 59 Ω for the nominally 50 Ω load resistor. The contact resistance associated with the interface between the annealed Au and the YBCO was measured to be 8.0×10^{-6} Ω-cm^2 at 75 K, also an acceptable value, and found to be ohmic (linear I-V curve). In spite of the problems with the degraded YBCO, this fabrication run and the associated measurements indicated that the concept of an integrated thin-film load resistor was a valid and realizable one. The YBCO transmission lines from the output connectors to the terminations themselves were therefore lossier than desired and this might, in principle, produce higher return losses when measuring the performance of the terminations. However, these were only a few millimeters long and so their effect on the measurements is expected to have been negligible.

- Fabrication of First Two Wafers for HTSSE-II Filters*

The wafer processing techniques being developed under this program were evaluated and further refined by using the HTSSE-II filters as test vehicles. Based on the results of the thin-film load fabrication run, a set of seven masks for the four channels in a channelized filterbank for HTSSE-II was designed at Westinghouse STC and fabricated by Micro Mask, Inc. The layout for the channel 1 filter, transition chips for interconnecting filter channels, and associated test patterns are shown in Figure 4. An expanded view of the dc test patterns that appear in this layout is given in Figure 5. In order to avoid trapping photoresist beneath the contact Au (as occurred for the thin-film

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*The design, layout, and mask fabrication for the filters were supported by NRL as part of the HTSSE-II program, while the process development was part of the ARPA/ONR program, including development of the test patterns.

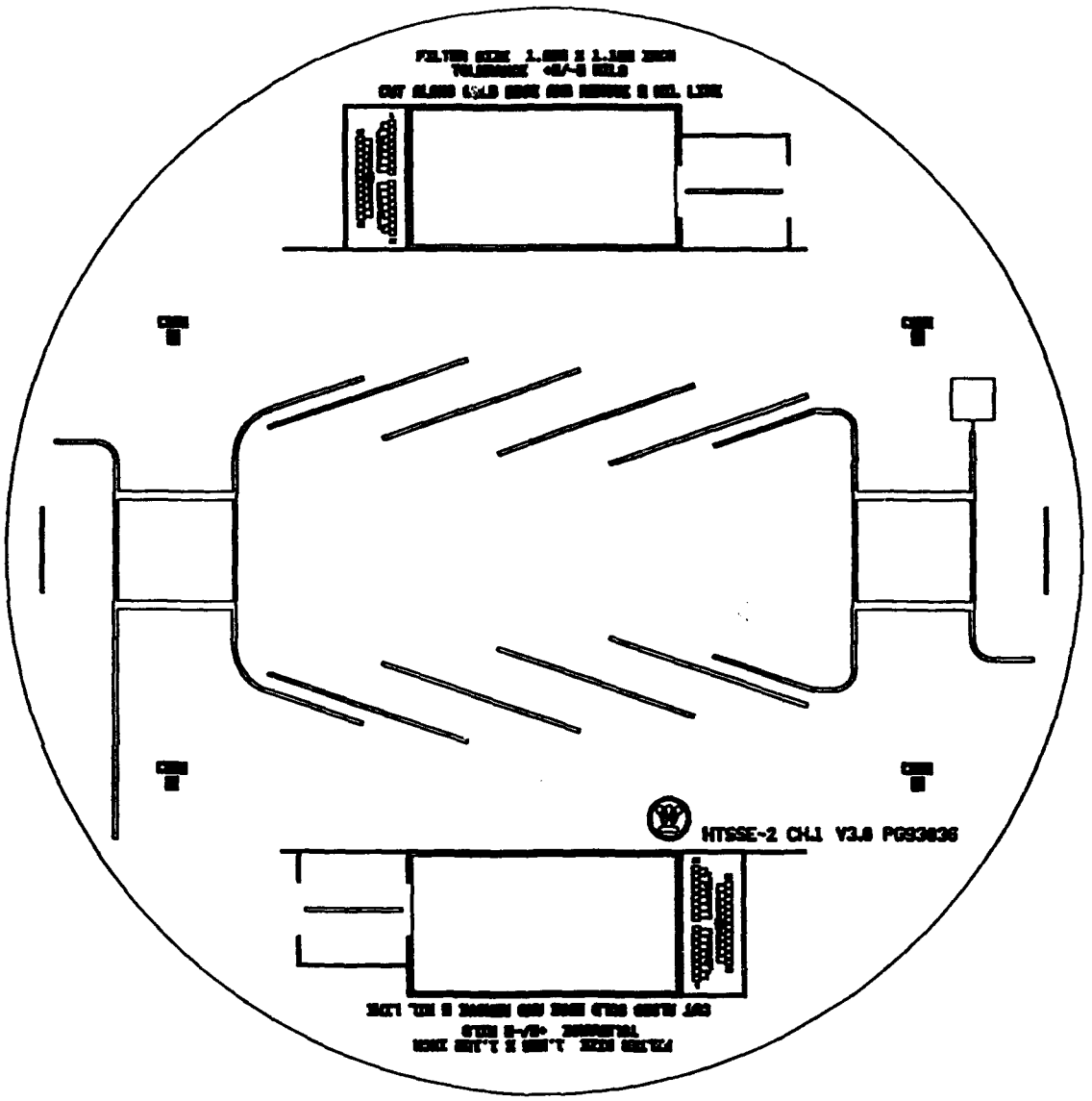

Figure 4. Diagram of layout of channel 1 filter (center) including the thin-film load structure (right), transition chips to facilitate connection of filter channels within a common package (lower left and upper right chips), test pieces for measurement of surface resistance after processing (two blank rectangular chips at top and bottom), and test patterns for measuring dc properties of YBCO and the thin-film Mo/Ti resistors (lower right and upper left chips) on a two-inch wafer.

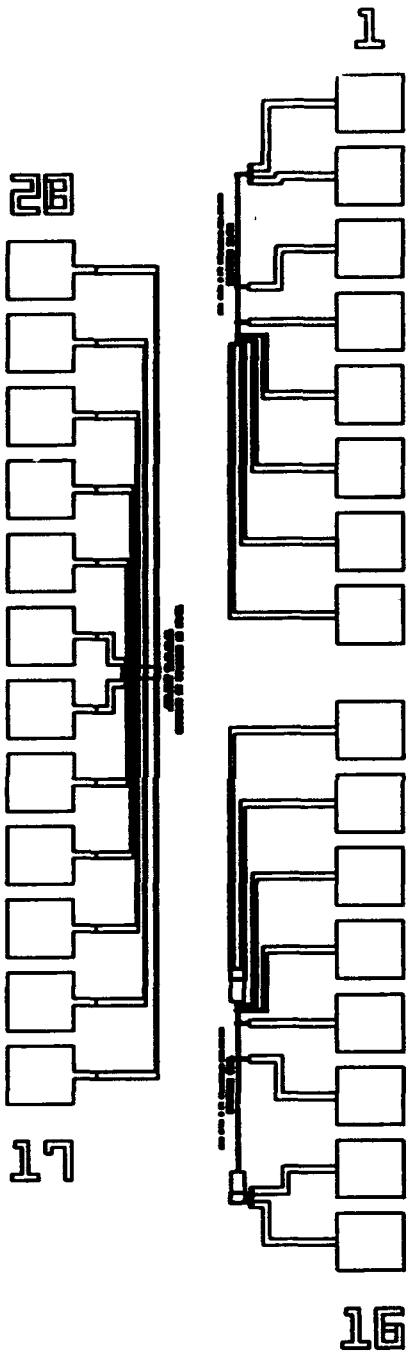

Figure 5. Expanded view of dc test patterns for measuring sheet resistance of Mo/Ti resistor at room temperature and at 77 K (upper right), sheet resistance at room temperature of YBCO and critical temperature and critical current density of YBCO at 77 K (lower right), and contact resistance between annealed Au and YBCO at 77 K (left).

load run), all isolated photoresist islands were eliminated from the contact mask level. Only the essential contacts themselves and the alignment marks remained on this mask.

The process sequence used in this fabrication is detailed in Table 2. It is similar to that employed in the thin-film load fabrication, except that the deposition of the ground plane by sputtering and plating is now the second major step in the process instead of the last step. In order to avoid breakdown of the photoresist layer which protects the front (YBCO) side of the wafer during plating, the plating time was reduced from 60 minutes to 30 minutes and the plating current was increased from 10 mA to 50 mA. This gives a plated Au thickness of ≈ 4 μm.

The most important parameter for the successful fabrication of a YBCO filter is the surface resistance. This parameter, measured at 77 K and normalized to 10 GHz, must be less than 5 mΩ. As long as the YBCO film is unpatterned, the surface resistance can be measured using a cavity resonator (end-wall replacement technique). Referring to Table 2, this means that the surface resistance can be monitored through the contact anneal step and through the ground plane plating step, arguably the steps most likely to cause degradation in the surface resistance. In addition, upon completion of the processing the wafer is sawed into its respective chips, including two 1/4" × 1/2" rectangles of unpatterned YBCO (Figure 4). These rectangular pieces can be placed in a parallel plate resonator to determine the surface resistance after the processing is complete.

Two substrates, each comprising a $LaAlO_3$ wafer (0.05 cm thick) on which an epitaxial layer of YBCO (0.4 μm thick) had been grown by off-axis sputtering at Westinghouse STC, have undergone the process sequence summarized in Table 2 and have been diced into chips. Surface resistance measurements were made at various steps in the process. Within experimental error, R_S was unaffected by the process and both wafers emerged from the entire process sequence with quite low values of surface resistance (0.7 mΩ and 1.4 mΩ), thereby demonstrating the ability of the process to preserve low values of surface resistance. There was no physical evidence of degradation to the YBCO surface, suggesting that the protective photoresist layer did not succumb to

Table 2. Process Sequence for HTS Filter

Mask	Description	Material	Thickness	Process
1	Contact to YBCO	Au	200 nm	Lift-off
	Contact anneal	Au on YBCO	n/a	550°C ramp in O_2
none	Ground plane base	Cr/Au	20/200 nm	Sputter
	Ground plane thick metal	Au	4 μm	Plate
2	Filter	YBCO	400 nm	Ion Mill
3	Resistor	Mo/Ti	76/10 nm	Lift-off
4	Capacitor and contact pads	Cr/Au	20/200 nm	Lift-off

Note:

- Substrate is 2-inch diameter $LaAlO_3$, 20 mils thick.
- Surface resistance at 77 K and 10 GHz is measured for starting YBCO film and after several of the first four steps above (until YBCO is patterned).
- Minimum feature size in filter: 10 μm (resistor width).
- Test patterns ($R_{surface}$, R_{sheet}, $R_{contact}$, T_c, J_c) are included on mask set.
- Wafers: W93-019 and W93-022.

Table 3. Results of Test Chip for Filter Fabrication

Run Filter-1

Wafer W93-019

YBCO Film (nominally 10 μm wide and 0.4 μm thick):
Sheet resistance at room temperature: 7.5 Ω/□ (300 μΩ-cm)
Critical temperature after four-mask level process: 87.0 K
Critical current at 77 K: 42 mA (1.0×10^6 A/cm^2)

Mo/Ti Resistor (nominally 760 Å/100 Å from Nordiko 2000):
Sheet resistance at room temperature: 2.31 Ω/□
Sheet resistance at 77 K: 1.40 Ω/□
Ratio (RT/LN) of sheet resistance: 1.65

Contact Resistance of Au annealed into YBCO:
Au annealing conditions: ramp to 550°C in 1 hour, then turn furnace off (flowing O_2)
Size of contact stripe: 10 μm × 50 μm
Contact is ohmic (linear I-V) up to 62 mA
Contact resistance at 77 K: 1.0 Ω/contact (1.0×10^{-6} Ω-cm^2)

the plating bath during the reduced (30 minute) plating time. Results of dc measurements from the test chip (Figure 5) for wafer W93-019 are listed in Table 3. All parameters are on-target, reinforcing the indication from surface resistance measurements that the YBCO remains of high quality In addition, the Au/YBCO interface has low contact resistance (1.0×10^{-6} Ω-cm^2) and the Mo/Ti resistor material has acceptable sheet resistance at 77 K (1.40 Ω/□). Measurements of the channel 1 and channel 2 filter characteristics at 77 K for these two wafers will be included in the next report.

- Integrated Packaging

The last report explained some of the package concepts being developed for the channelizer, principally the use of niobium as the thermal expansion matched carrier material for substrate mounting, and the use of spring contacts instead of indium-based solders to secure and contact the carrier to the aluminum package housing. Designs incorporating these features were completed during the current reporting period, and machining of parts was begun. The complexity of the package parts is accommodated by using numerically controlled milling. Identical packages will be used for the channelizers being fabricated for both programs, and this commonality results in cost and time savings.

Delay Lines

- Indium Diffusion Barrier Experiments

Further experiments on the need to use In diffusion barriers have revealed no contamination of the YBCO through the annealed Au contact layer. A set of rectangular $LaAlO_3$ samples 1/2" × 1/4" with YBCO on one side was coated on the same side with 200 nm of sputtered Au. The samples were then annealed in flowing oxygen for 1 hour at 550° C in order to provide a low contact resistance between the gold and the YBCO. These samples were subsequently subjected to a simulated In soldering to a Nb carrier, using temperatures 10 to 20° C higher than the actual soldering process temperature of 150° C. Using a separate sample of the same size, a microstrip resonator was defined on

the YBCO by ion milling. By laying this sample with the resonator side in contact with the bare side of the test YBCO/Au samples, the quality factor of the microstrip resonators was measured, with the YBCO/Au as the ground plane. This measurement was done before and after the YBCO/Au side was subjected to the In soldering process. In both cases a Q of several thousand was measured for the two samples processed. Inductive T_c measurements were also performed, which showed no degradation at all from the contact with In through the gold layer at the process temperature. We conclude then that the contact gold layer is sufficient to prevent degradation of the YBCO by the In at the processing temperature of 150°C. This will be tested in an actual delay line in the next reporting period.

- Fabrication and Packaging

A delay line package design was completed which incorporates features for obtaining and holding the required alignment of top and bottom mirror image spirals. This alignment procedure entails registration of fiducial markings on the top and bottom substrates which are photolithographically defined at the same time as the delay line spiral itself. To allow these markings to be viewed for the alignment, small holes in the ground plane layers on the back sides of each substrate are also photolithographically produced, these holes being in registration with the fiducial marks on the front sides. The marks can thus be viewed through the transparent substrate to allow the required registration to be accomplished. Mating holes in the substrate carriers allow an unobstructed optical path, and an alignment jig allows both translation and rotation of one of the substrate carriers relative to the other, while pressure is maintained to keep the substrates in good contact. When alignment is achieved, pins connecting the carriers will be epoxied in place to fix the carriers from moving in translation, and substrate contact pressure will be maintained by nuts and bellville washers on these pins. Ground plane contact between the back sides of the substrates will be accomplished by a spring contact spiral at the periphery of the

substrates, between the carriers. The aligned assembly will then be inserted into an aluminum housing in a similar manner to the filter carrier insertion into the channelizer.

Parts are in process of machining for the delay lines, and a test of the whole alignment procedure and of the delay line itself will occur in the next quarter.

TASK 3.1: PVD MULTILAYER FILM FABRICATION

The two subtasks scheduled for this reporting period required delivery of YBCO films on both sides of two-inch diameter substrates to Task 2.2, and development of a multilayer deposition capability on four-inch wafers.

A production schedule was charted in April, 1993, for this program and HTSSE II which called for approximately 80 two-inch diameter wafers to be coated with 400 nm thick YBCO films on one or both sides between May and October, 1993. So far, film production has stayed ahead of fabrication requirements. As mentioned in previous reports, the only variable in the production process that has prevented a 100% film yield is the homogeneity of YBCO sputtering targets. The problem encountered with approximately one out of five targets is that the plasma becomes concentrated on a target inhomogeneity and burns a hole in the target during its first use. The evaporated material from such a hole is not stoichiometric and films produced from such targets must be stripped off and the substrate recycled. During this quarter, we met with the two primary vendors of YBCO targets to discuss our requirements and reduce the number of targets returned to them. Several new types of targets made from different starting powders were obtained from each vendor and will be evaluated in December, 1993.

As production of filter channels and delay lines proceeded during this quarter, spot checks of R_S were discontinued in favor of R_S measurements made during processing of devices to ensure that process steps did not degrade film quality. In the case of filter channels, the completed device contained test chips on which R_S could be measured. These measurements provided sufficient feedback to the film production process to show that R_S-qualified films were being supplied.

As in the previous quarter, a very low level of effort was expended in the development of YBCO-coated four-inch wafers using a new sputtering chamber built to a Westinghouse design by Nordiko Ltd., which can accommodate 2, 3, or 4-inch wafers. Although modifications to the thermal design had reduced the heater power needed to maintain the desired substrate temperature from an initial value of 70% to less than 30% of the heater's 2.6 kW maximum, rotary feedthroughs in the vicinity of the heater were overheating during long deposition sequences. Nordiko re-designed these feedthroughs so they are water-cooled, rebuilt them, and delivered them to Westinghouse in August, 1993. The modified feedthroughs were found to be poorly designed, leading to vacuum leaks and loss of the ability to monitor wafer temperature during growth. Nordiko has agreed to redesign and build suitable feedthroughs.

TASK 3.2: MOCVD MULTILAYER FILM FABRICATION

Work under this task was performed at EMCORE on YBCO film growth, at Northwestern University on the development of new Ba precursors for YBCO and growth of epitaxial insulating films, and at Westinghouse STC where measurements were made of the rf surface resistance of YBCO films. However, during this reporting period no YBCO films were delivered to Westinghouse so no R_S measurements were performed.

Northwestern University has fabricated three generations of Ba precursors during the course of this program. Film growth and Ba transport were demonstrated with the third-generation precursors, bis(tri-butylcyclo-pentadienyl)barium, $(Cp^tBu_3)_2Ba$, and bis(di-butylcyclo-pentadienyl)barium, $(Cp^tBu_2)_2Ba$. These precursors appear to successfully address all of the requirements for MOCVD of Ba compounds and represent a successful conclusion to this part of the program. A preprint is attached as Appendix A.

TASK 3.3: RF CHARACTERIZATION OF FILM PROPERTIES

Three techniques continue to be used for R_S measurements. The most important one for this program is a cylindrical copper cavity designed for two-inch diameter wafers

(end-wall replacement technique). Some refinements to the measurement technique were implemented during this reporting period to eliminate potential degradation of the sample by scratches, dust, or grease.

The other technique for R_S measurement of 2-inch wafers is the dielectric resonator used in the STALO program. Although it is not preferred to the cavity with end-wall replacement for screening films, it does provide feedback to the same deposition process as used for this program.

The third technique is a parallel-plate resonator using a pair of 1/2 inch × 1/4 inch unpatterned films. When there is room on a wafer that is processed for other purposes (for example, tests of thin-film loads), chips of this size are cut from the wafer after processing is complete and measured to determine whether any change in R_S occurred due to processing.

TASK 5.0: SWITCHED FILTERBANK

The schedule shown below is for the development and testing of the etched back FET switch which is the primary product of the first phase of the flow-through switched filterbank add-on to the current program. It indicates that if the first switch run is successful we will be well ahead of schedule.

DESIGN COMPLETED	12/03/93
MASK COMPLETED	12/17/93
1ST PROCESS RUN COMPLETED	2/28/94
TESTING COMPLETED	3/14/94
REDESIGN, NEW FABRICATION & TEST (IF NECESSARY)	6/14/94

PROBLEMS ENCOUNTERED AND/OR ANTICIPATED

Although the start date of this program was July 24, 1991 with the approval of anticipatory spending, the contract was not signed until September 30, 1991 when the first increment of funding was received. The work effort was slowed at DARPA's request to stretch the FY92 funding through 12/31/92. However, FY93 funds were not received until March 30, 1993. These funding limitations will place the program at least six months behind schedule.

FISCAL STATUS

Amount currently provided	$3,516,013
Expenditures and commitments through 10/24/93:	2,965,184 *
Funds required to complete:	2,999,223
FY94 funds required:	2,300,000

*Includes $437,400 committed to subcontractors and purchase orders.